CDB5451A

CDB5451A Evaluation Board and Software

Features

- Direct Shunt Sensor and Current Transformer Interface for 3-Phase Power
- On-Board Voltage Reference
- On-board crystal for XIN
- Digital Interface to PC
- Lab Windows/CVI™ Evaluation Software
  - Real-Time RMS calculation
  - Fast Fourier Transform (FFT) Analysis
  - Time Domain Analysis
  - Noise Histogram Analysis

General Description

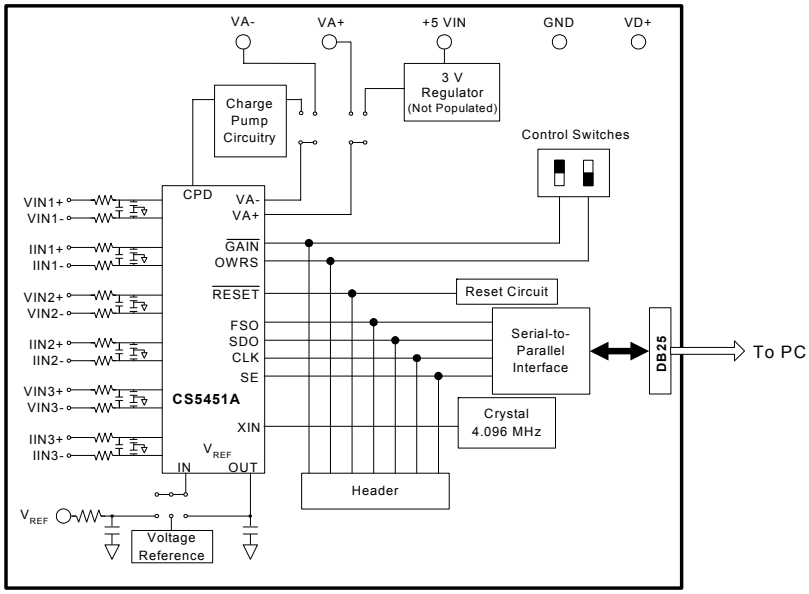
The CDB5451A is an inexpensive tool designed to evaluate the functionality/performance of the CS5451A 6-channel A/D Converter. In addition to this data sheet, the CS5451A Data Sheet is required in conjunction with the CDB5451A Evaluation Board.

Six terminal block connectors serve as inputs to the CS5451A's six analog input pairs. The CDB5451A includes an optional voltage reference source for CS5451A. A 4.096MHz crystal is provided as a source for the CS5451A XIN pin, or an external clock source can be supplied by the user. Digital output data from the CS5451A is transferred to the user's IBM-compatible PC via the included 25-pin parallel port cable.

The CDB5451A includes PC software, allowing the user to perform data capture (includes option for time domain analysis, histogram analysis, and frequency domain analysis). The software also allows real-time RMS calculation/analysis to be performed simultaneously on all six channels.

ORDERING INFORMATION

CDB5451A Evaluation Board



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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1. INTRODUCTION

The CDB5451A Evaluation Board demonstrates the performance of the CS5451A 6-channel A/D converter.

The CDB5451A evaluation board provides a quick means of evaluating the CS5451A. Analysis software supplied with the CDB5451A allows the user to observe the CS5451A's digital output data on the user's PC monitor. The PC software allows the user to quantify the device's performance in the time-domain and frequency domain. The user can save raw data from the CS5451A to a data file, which allows to user to analyze performance with other tools that may be preferable to the user.

1.1 CS5451A

The CS5451A is a highly integrated Six-Channel Delta-Sigma Analog-to-Digital Converter (ADC) developed for three-phase power/energy metering applications. However the CS5451A has other potential uses in other data acquisition applications, particularly in motor/servo control applications that require very high precision. The CS5451A combines six delta-sigma modulators with decimation filters, along with a master-mode serial interface on a single-chip device. The CS5451A was designed for the purpose of performing the A/D conversion operations required at the front-end of a digital 3-phase metering system. The six ADC channels can be thought of as three pairs of voltage/current-channel ADC's in a digital 3-phase power metering application.

The CS5451A contains one three-channel programmable gain amplifier (PGA) for the three current input channels. The PGA sets the maximum input levels of the all three current channels at ±800 mV DC (for gain = 1x) or ±40 mV DC (for gain = 20x). The voltage channels have only the 1x gain setting, and so the range of input levels on the voltage channels is ±800 mV DC.

Additional features of CS5451A include a charge pump driver, on-chip 1.2 V reference, and a digital input that can select between two different output word rates. (The two output word rates are equal to XIN/2048 and XIN/1024.)

The CS5451A requires a 1.2 V reference input on VREFIN. The $\Delta\Sigma$ modulators and high rate digital filters allow the user to measure instantaneous voltage and current at an output word rate of 4 kHz (or 2000 kHz, depending on the state of the OWRS pin) when a 4.096 MHz clock source is used.

1.2 Data Flow on Evaluation Board

The output serial bit-stream from the CS5451A is shifted into an 8-bit latch circuit so that it can be quickly ported to the DB25 connector. From this connector, the data can be sent through the provided 25-pin printer cable to the parallel port of the user's IBM-compatible PC (the PC must run under Windows '95/'98/2000 operating system).

Once the 8-bit segments of data are ported to the user's PC, the LabWindows software (included with this kit) will re-segment the data into the appropriate 16-bit word format for each of the CS5451A's six data channels. The data is sent quickly to the user's PC, which allows the software to perform various data processing and graphical illustrations on the digital output data. This includes real-time RMS, variance, and standard deviation calculations for all six channels. The output data from each channel can be plotted on-screen in the time domain or in the frequency domain. A histogram function is also included to help the user to evaluate the noise characteristics of each channel. The software can also calculate the mean and standard deviation of the output codes for all six channels. This feature allows the user to scrutinize the variation of the A/D converters if the user applies constant DC voltage levels to the inputs. RMS calculation is also provided to assist in the quick analysis AC input signals.

2. HARDWARE

2.1 Evaluation Board Description

The CDB5451A board contains circuitry that will:

- Accept appropriate DC voltage levels from the user's +3V and/or +5V power supplies, and direct this power to the VA+, VD+, VA- and DGND pins of the CS5451A.
- Direct the six analog input signals to the six input pairs of the CS5451A.
- Supply necessary voltage reference input for the CS5451A's VREFIN pin.
- Supply appropriate crystal/oscillator stimulus to the CS5451A's XIN pin.
- Direct the output driver signal from the CS5451A's charge-pump driver pin (CPD) which is used produce the negative power supply source for the CS5451A's VA- pin.
- Provide a reset switch that allows the user to set the CS5451A's $\overline{\text{RESET}}$ pin from logic "1" to logic "0".
- Provide two DIP switches which allow the user to set the logic levels on the CS5451A's $\overline{\text{GAIN}}$ and OWRS input pins.
- Detect and receive the data frame signal and digital serial output data signals from the CS5451A's FSO and SDO pins, and send this output data through the included parallel cable, and up to user's PC.

Several areas of blank proto-board space are provided so that, if desired, the user can interface their own electronic sensor equipment onto the board. The output from these sensors can be wired to the six nearby analog input terminal block connectors, which is then fed to the six analog input channels of the CS5451A. Examples of such sensors would include voltage and current transformers, shunt resistors, and resistor divider networks.

The next section of this document describes the various sections of the board. After this, operation of the PC software is described in detail.

2.2 Power Supply Connections

The CDB5451A can be used in several different power supply configurations. Table 1 shows the various possible power connections with the required jumper settings. There are various +3 V and +5 V options. The user must supply the +3V, +5V, GND, and sometimes -2V voltage levels needed to power the evaluation board.

2.2.1 Analog Power Supply

Referring to Figure 1, the A+ post supplies power to the positive analog power input pin (VA+) of the CS5451A. This post also supplies power to the LT1004 voltage reference (D3) and the optional +3V regulator (U5). If HDR9 is set to the "A-" setting, the A- post can supply the required negative voltage to the VA- pin of the CS5451A.

Note that the evaluation board contains the footprints and connectivity which allows the user to install a LM317 voltage regulator (U5), which can be used to create +3 V from a +5 V supply. This option is useful if the user wants to interface the evaluation board to another board that can only operate from a +5V supply. With HDR17 set to "+5V_IN", one single +5 V supply can be used to provide both the +5 V power to a microcontroller and/or other devices, as well as +3 V for the CDB5451A board. The included schematic diagram shows the circuitry for the +5V regulator circuitry inside a box with dashed lines. These components are not populated when the board is shipped from the factory, but the user can install these components if desired.

2.2.2 Digital Power Supply

The A+ post can be used to supply both the analog power (to CS5451A VA+ pin) as well as the digital power (to CS5451A VD+ pin). However if a separate supply voltage is desired for the digital power supply, the "VD+" banana connector post can be used to independently supply a separate digital power supply to the input of the CS5451A (VD+ pin), the 4.096 MHz oscillator (U1), and circuitry for the parallel port interface. This is controlled by the setting on HDR18.

The user should note that the CS5451A can operate with a digital supply voltage of either +3V or

+5V. This voltage is defined as the voltage presented across VD+ and DGND.

2.2.3 Charge Pump Options

The output from CS5451A's charge-pump driver pin (CPD) can be used to generate a -2V supply when the proper jumper settings are selected on HDR9. This -2V supply can be used as the negative power supply connection for the CS5451A's VA- pin. Referring to Figure 1, circuitry for a charge-pump circuit is included on-board. The charge pump circuit consists of capacitors C11, C12, and C36, and diodes D1 and D2.

As an alternative to using the charge pump circuit, the user can supply an off-board -2V DC power source to the "A-" banana connector. This option is controlled by the setting on HDR9.

2.3 Eval Board Control - Headers/Switches

Table 2 lists the various adjustable headers and switches on the CDB5451A Evaluation Board, as well as their default settings (as shipped from the factory). The header settings can be adjusted by the user to select various options on the evaluation board. These options are described further in the following paragraphs.

2.3.1 Analog Inputs

Refer to Figure 2. The settings on the 12 analog input headers (2 headers per channel) which are designated as HDR1 up to HDR8, and HDR10 up to HDR13, determine which inputs will carry a signal, and which inputs may be grounded. They can be configured to accept either a single-ended or

Power Supplies		Power Post Connections							
Analog	Digital	A+	A-	GND	D+	+5 V_IN	HDR9	HDR17	HDR18
+3	+3	+3	-2	0	+3	NC	A- CPD	+5V_IN A+	VD+ V+
+3	+3	+3	-2	0	NC	NC	A- CPD	+5V_IN A+	VD+ V+
+3	+3	+3	NC	0	+3	NC	A- CPD	+5V_IN A+	VD+ V+
+3	+3	+3	NC	0	NC	NC	A- CPD	+5V_IN A+	VD+ V+
+3	+3	NC	-2	0	NC	+5	A- CPD	+5V_IN A+	VD+ V+
+3	+3	NC	NC	0	NC	+5	A- CPD	+5V_IN A+	VD+ V+
+3	+5	+3	-2	0	+5	NC	A- CPD	+5V_IN A+	VD+ V+
+3	+5	+3	NC	0	+5	NC	A- CPD	+5V_IN A+	VD+ V+
+3	+5	NC	-2	0	+5	+5	A- CPD	+5V_IN A+	VD+ V+
+3	+5	NC	NC	0	+5	+5	A- CPD	+5V_IN A+	VD+ V+
+5	+3	+5	0	+2	+5	NC	A- CPD	+5V_IN A+	VD+ V+

Table 1. Power Supply Connections

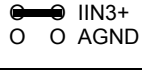
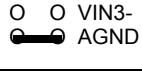
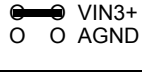
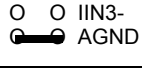
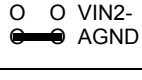
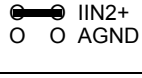
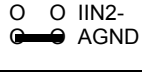
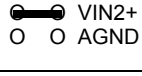
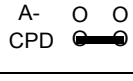
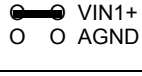
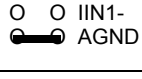
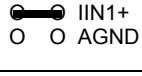
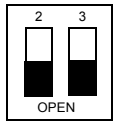
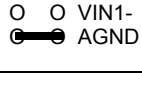
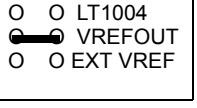
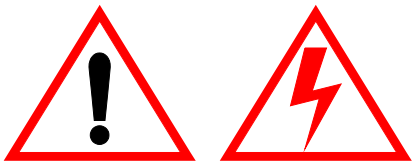
Name	Function Description	Default Setting	Default Jumpers
HDR1	Used to switch IIN3+ on the CS5451A between J2 and AGND.	IIN3+ Set to BNC J2	
HDR2	Used to switch VIN3- on the CS5451A between J3 and AGND.	VIN3- Set to BNC J3	
HDR3	Used to switch VIN3+ on the CS5451A between J1 and AGND.	VIN3- Set to BNC J1	
HDR4	Used to switch IIN3- on the CS5451A between J4 and AGND.	IIN3- Set to BNC J4	
HDR5	Used to switch VIN2- on the CS5451A between J6 and AGND.	VIN2- Set to BNC J6	
HDR6	Used to switch IIN2+ on the CS5451A between J7 and AGND.	IIN2+ Set to BNC J7	
HDR7	Used to switch IIN2- on the CS5451A between J5 and AGND.	IIN2+ Set to BNC J5	
HDR8	Used to switch VIN2+ on the CS5451A between J8 and AGND.	VIN2+ Set to BNC J8	
HDR9	Used to switch between external VA- and on-board CS5451A charge-pump circuit, CPD	CPD active	
HDR10	Used to switch VIN1+ on the CS5451A between J9 and AGND.	VIN1+ Set to BNC J9	
HDR11	Used to switch IIN1- on the CS5451A between J12 and AGND.	IIN1- Set to BNC J12	
HDR12	Used to switch IIN1+ on the CS5451A between J10 and AGND.	IIN1- Set to BNC J10	
SW1	S1-1 sets logic level on CS5451A OWRS input pin S1-2 sets logic level on CS5451A $\overline{\text{GAIN}}$ input pin	SW1-2 Open (XIN/1024) SW1-1 Open ($\overline{\text{GAIN}}$=x1)	
HDR13	Used to switch VIN1- on the CS5451A between J11 and AGND.	VIN1- Set to BNC J11	
HDR14	Used to switch the VREFIN from external VREF post connector, to the on board LT1004 reference, or to the on-chip reference VREFOUT. Refer to Table 3.	VREFIN Set to on-chip reference VREFOUT	

Table 2. Default Header Settings

Name	Function Description	Default Setting	Default Jumpers
HDR15	Controls the source for the CS5451A XIN clock input.	Set to on-board 4.000 MHz crystal (U1).	O O EXT XIN O O DGND 4.0096 MHz OSC
HDR16	This header should always be shorted.	Short this header	
HDR17	Determines whether the main analog supply will be powered from the A- post, or from the regulated 3V voltage (generated from the +5V_IN) post input.	Set to A-	O O +5V_IN A+
HDR18	Choose whether the digital circuitry will be powered by main analog supply, or powered by separate digital supply (through VD+ post).	Set to main analog supply	VD+ O O V+

Table 2. Default Header Settings (Continued)

differential signal. Using voltage channel #1 as an example (see Figure 2), note that HDR10 sets the input to the positive side of the first voltage channel input (VIN1+ pin). HDR13 sets the input to the negative side of the first voltage channel input (VIN1- pin). In a single-ended input configuration, HDR13 would be set to the "AGND" setting, and HDR10 would be set to "VIN1+" and would conduct the single-ended signal. In a differential input configuration, HDR13 would be set to "VIN1-" and HDR10 would be set to "VIN1+" and this pair of inputs would form the differential input pair into the VIN1+ and VIN1- pins of the CS5451A.



WARNING: DANGER! *One of the possible applications for the CS5451A includes data acquisition for a power metering system. However, the user should not attempt to directly connect any lead from a high-voltage power line to the evaluation board inputs, even if the current/voltage levels are gain reduced by resistive dividers and/or shunts. Because the ground terminal of the parallel cable (from the PC) is near or at earth ground potential, the ground node on the evaluation board will also be forced to earth ground potential. Serious damage and even personal injury can occur if a "hot" voltage main is connected to any point on the evaluation board, including the analog input connectors. Such power line signals must be isolated by current/voltage transformers and reduced in magnitude before they can be safely applied to the evaluation board.*

Several patch-circuit areas are provided near the voltage/current input headers, in case the user wants to connect special sensor circuitry to the analog inputs (such as transformers, shunt resistors, etc., for monitoring a 3-phase power line). For each of the three channels, a Shunt Resistor or Current Transformer can be mounted in these areas and connections can be made to the individual current-channel input pairs. Likewise, for each of the three voltage channels, a Voltage Divider or Voltage Transformer can be inserted to drive the CS5451A's three voltage input pairs. Note from Figure 2 that a simple R-C network filters each sensor's output to reduce any noise that might be coupled into the input leads. The 3 dB corner of the filter is approximately 50 kHz differential and common mode.

Other header options listed in Table 2 allow the user to set the source of the input clock signal and the source of the voltage reference (VREFIN) input, etc. The voltage reference options and clock input options are discussed next.

2.3.2 Voltage Reference Input

To supply the CS5451A with a suitable 1.2 V voltage reference input at the VREFIN pin, the evaluation board provides three voltage reference options: on-chip, on-board, and external. See HDR14 as shown in Figure 1. Table 3 illustrates the available voltage reference settings for HDR14. With HDR14's jumpers in position "VRE-

Reference	Description	HDR14
LT1004	Select on board LT1004 Reference (5 ppm/°C)	LT1004 O O VREFOUT O O EXT VREF
VREFOUT	Select reference supplied from CS5451A VREFOUT pin	O O LT1004 VREFOUT O O EXT VREF
EXTVREF	Select external reference	O O LT1004 O O VREFOUT EXT VREF

Table 3. Reference Selection

FOUT," the CS5451A's on-chip reference provides 1.2 volts. With HDR14 set to position "LT1004," the LT1004 provides 1.23 volts (the LT1004 temperature drift is typically 50 ppm/°C). By setting HDR14's jumpers to position "EXT VREF," the user can supply an external voltage reference to J16 connector post (VREF) and AGND inputs.

2.3.3 Clock Source for XIN

A 4.000 MHz crystal is provided to drive the XIN input of the CS5451A. (See Figure 1.) However, the user has the option to provide an external oscillator signal for XIN, by switching the setting of HDR15.

2.3.4 S1 DIP Switch

Referring to Figure 3, the two single-pole single-throw switches on SW1 DIP switch should be used to control the logic settings on the CS5451A's OWRS pin and $\overline{\text{GAIN}}$ pin. When these SW1 switches are set to "OPEN" the corresponding pin on CS5451A is set to D+ potential, which creates a logic-high state. When the user closes either of these SW1 switches, the corresponding pin on CS5451A is grounded, which creates a logic-low state on the pin.

2.3.5 Reset Circuit

Circuitry has been provided which allows the user to execute a hardware reset on the CS5451A. (See Figure 3). By pressing on the S1 switch, the $\overline{\text{RESET}}$ pin on the CS5451A will be held low until the switch is released.

2.3.6 External Signal In/Out Header

Note that HDR16 is included on the CDB5451A Evaluation Board as a header that is normally left unconnected. This header provides a way for the user to interface the CDB5451A Evaluation Board to other prototype boards, calibrators, logic analyzers, other peripherals, etc. in order to further evaluate the CS5451A device and/or to use the evaluation board as a platform for the prototype development of a digital power meter solution. However, please note that the CDB5451A Evaluation Board is not intended to be integrated directly into a commercial power meter. The layout of the board is not optimized for practical power metering situations.

2.3.7 Serial-to-Parallel Interface

Glue-logic on the evaluation board converts the CS5451A serial data into 8-bit segments (bytes). The bytes are sent to the DB25 connector (J17), and then through the standard printer cable to the user's PC. This section briefly describes the operation of the digital circuitry on the CDB5451A that provides the 8-bit parallel data to the PC. Refer to Figure 3.

The user should recall from CS5451A Data Sheet that the serial interface on the CS5451A device is a "master-mode" interface, which means that the device provides the clock. Once the CS5451A is powered on, the SCLK pin produces a clock signal, and data is sent out on the SDO pin of the device. When the evaluation software is instructed (by the user) to acquire data through the parallel interface, a two-step process is performed: First the software synchronizes itself to the frame rate of the CS5451A, then the software acquires multiple frames of data from the CS5451A.

2.3.7.1. Synchronization

When the software is commanded to acquire data, the software will first synchronize itself to the frame rate of the CS5451A (see CS5451A Data Sheet). This is done by measuring the amount of time between rising and falling edges of the "BUSY" signal. (BUSY will change state every time the CS5451A issues eight SCLKs--See next section for a more detailed description.) By measuring this time period, the software can determine the idle period of the frame, which allows it to be prepared to collect a complete frame's worth of data when the next CS5451A frame is received. This acquisition sequence is described next.

2.3.7.2. Acquisition

Referring to Figure 3, the CS5451A's SCLK line is used to clock the 8-bit serial-in/parallel-out shift-register (U7) which accepts the serial data on SDO and shifts it into the 8 output bits QA-QG. The SCLK signal is also fed into the up/down counter U6 and after every 8 SCLKs, the "QC" pin of U6 will latch the QA-QG output bits of U6 into the 8-bit D-Flip-Flop (U3). While this is happening, the software monitors the "BUSY" signal (from the "QD" pin of U6). BUSY is the critical handshake signal. A rising *or* falling transition on BUSY indicates to the software that it is now time to collect another byte of data from the latched output on U3.

After sixteen SCLKs, the PC software has acquired two bytes (16 bits) which represents one data sample. The 4-bit up/down counter (U6) will roll over after every 16 SCLKs. (Note that U6 is cleared by the CS5451A's FSO signal at the beginning of each frame, which insures that the counter begins the frame in the correct state--cleared). This sequence, which lasts for 16 SCLKs, is performed a total of six times in order to obtain the six 16-bit words from the CS5451A.

After the last 16-bit word is acquired, the software recognizes that the end of a data frame has been reached, and it will continue to wait for the next transition on the "BUSY" line. This will not occur until the first 8 SCLKs of the next frame are sent from the CS5451A. Various other signals in Figure 3 (STRB, FEED, ACK, etc.) are not used during data capture and are only used for testing (internal use only).

2.3.8 Connecting the Eval Board to PC

The CDB5451A connects to the user's IBM-compatible PC with the included 25-pin parallel port cable. ***The user should not connect this cable between the CDB5451A and the parallel port on the PC until all of the header options in Table 2 have been set to appropriate settings and the user has applied power to the CDB5451A.*** The parallel cable attached to the CDB5451A Evaluation Board at J17. After connecting the parallel port cable between the PC and CDB5451A, the user should always actuate (press down on) the "RESET" switch (S1) at least one time before performing any other evaluation activities.

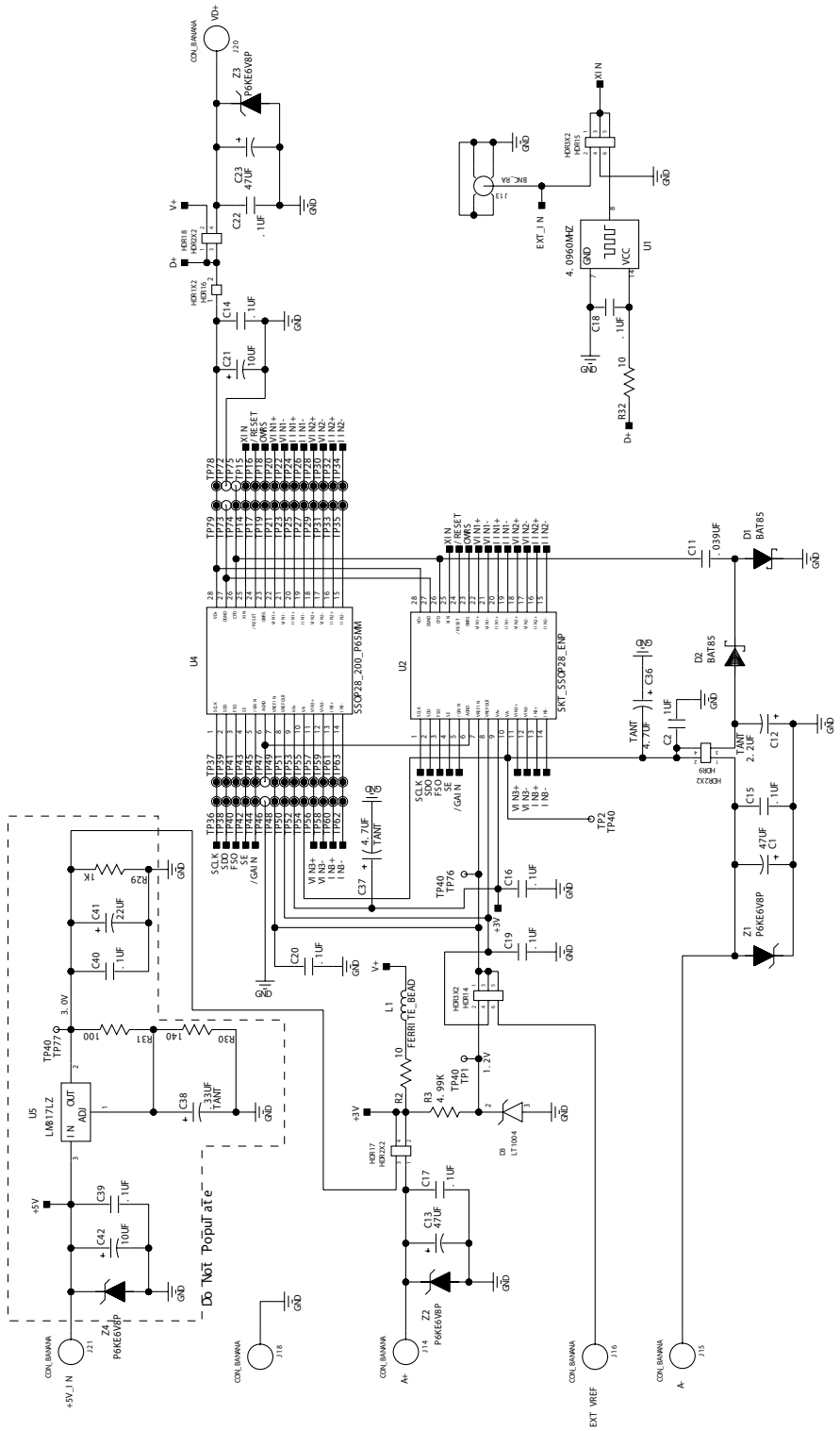


Figure 1. Power Supply, CS5451A, and Oscillator

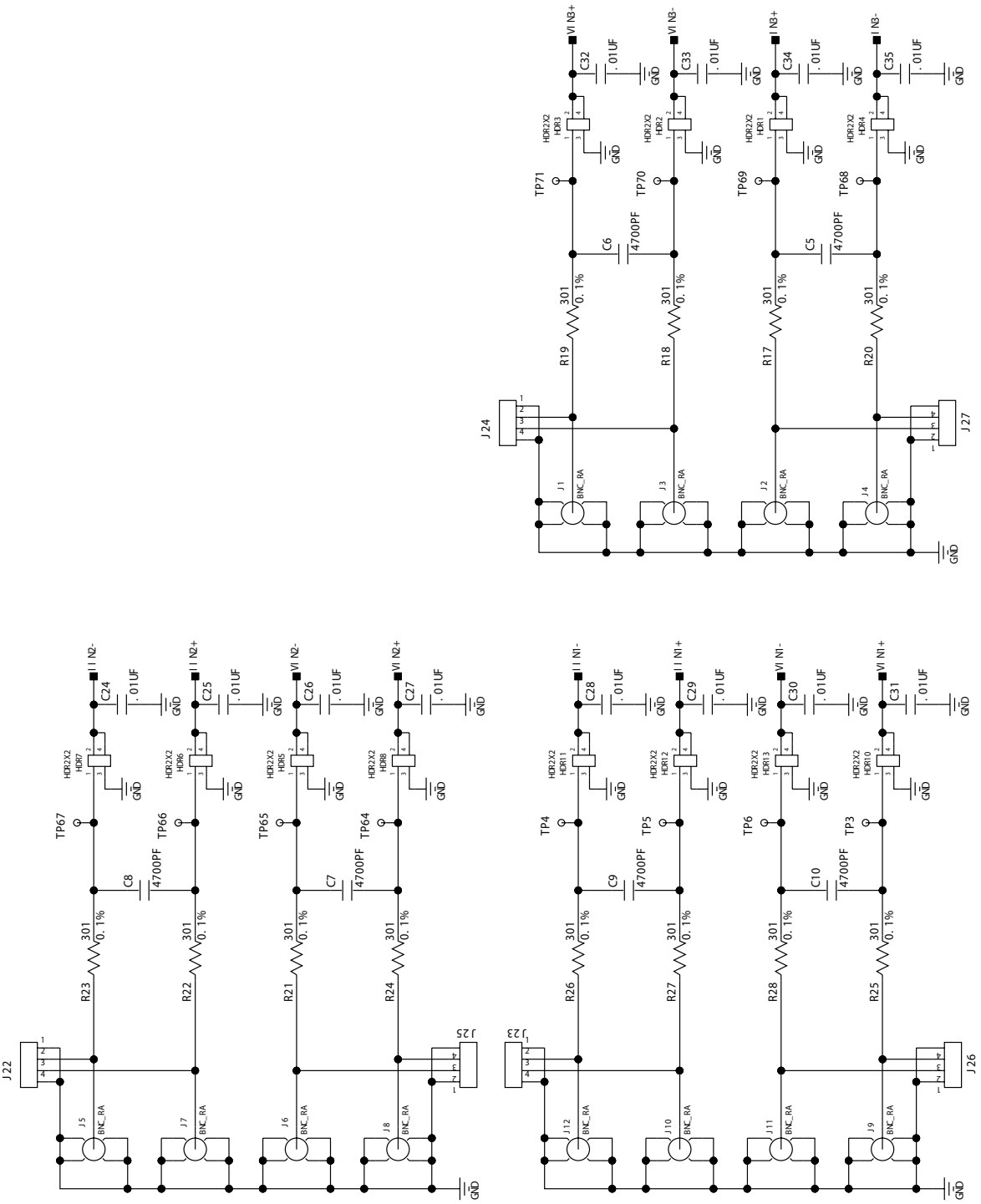


Figure 2. Analog Inputs

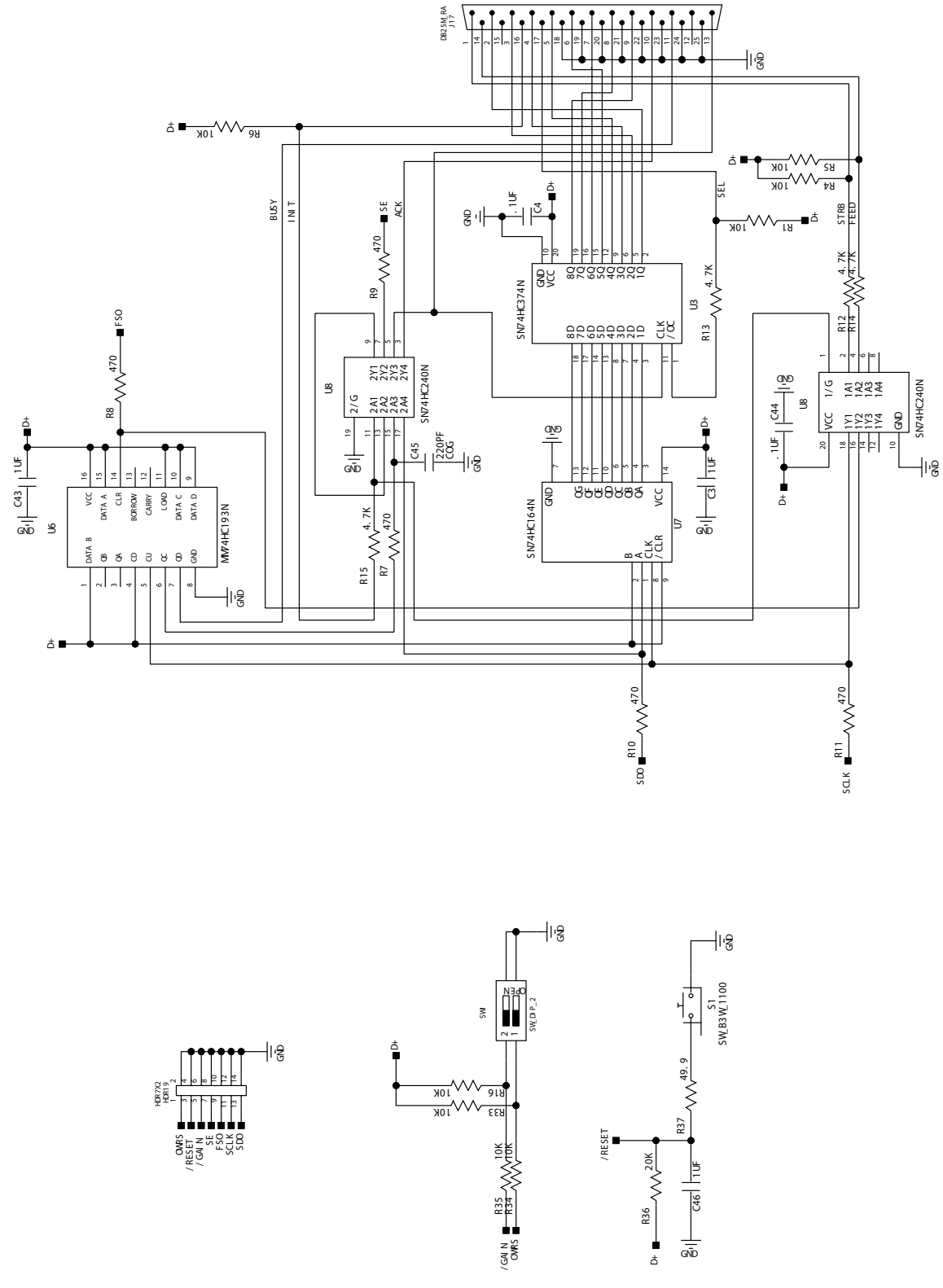


Figure 3. Digital Circuitry

3. SOFTWARE

The evaluation software was developed with Lab Windows/CVI™, a software development package from National Instruments. The software is designed to run under Windows 95™ or later, and requires about 3 MB of hard drive space (2 MB for the CVI Run-Time Engine™, and 1 MB for the evaluation software). Before installing the software, read the readme.txt file for any last minute updates or changes. More sophisticated analysis software can be developed by purchasing the development package from National Instruments (512-794-0100).

3.1 Installing the Software

Installation Procedure:

1) Turn on the PC, running Windows 95™ or later.
2) Insert the Installation CD into the PC.
3) Run the appropriate installer package (either instmsi.exe or instmsiw.exe, depending on the operating system). See the readme.txt file for more information.
4) Run EVL5451A.msi to begin installation.
5) During installation the user will be prompted to enter the directory in which to install the Lab-Windows CVI Run-Time Engine™. The Run-Time Engine™ manages executables created with Lab Windows/CVI™. If the default directory is acceptable, select OK and the Run-Time Engine™ will be installed there.
6) After the Run-Time Engine™ is installed, the user is prompted to enter the directory in which to install the CDB5451A software. Select OK to accept the default directory.
7) Once the program is installed, it can be run by double clicking on the EVL5451A icon, or through the Start menu.

Note: The software is written to run with 640 x 480 resolution; however, it will work with 1024 x 768 resolution. If the user interface seems to be a little small, the user might consider setting the display settings to 640 x 480. (640x480 was chosen to accommodate a variety of computers).

3.2 Running the Software

3.2.1 Getting Started

The CDB5451A Evaluation software allows the user to obtain, display, and save data that is acquired by the CS5451A chip. Before running the software, the first step is to make sure that all of the headers that are listed in Table 2 are set to an appropriate setting, the exact setting should be determined by the user. Next, with the user's DC power supplies still turned off, the user should connect the necessary power leads to the banana jack power connectors on the evaluation board. Refer to Table 1 for various acceptable power supply connection configurations. Then at this time the user should turn on their DC power supplies, which should apply power to the CDB5451A. Several test point locations are available on the evaluation board. The user can check these test points with a voltmeter, to make sure that the voltages at these test points are at the expected levels. When the user has verified that the power supply levels are constant, the user should connect the included 25-pin cable between J17 of the evaluation board and the parallel port on the user's PC. The user should then press down on the S1 "RESET" switch, and make sure to hold it down for at least ~0.5 seconds before releasing. Finally, the user can start the PC software. To start the software, double click on the EVAL5451A icon, or initiate through the Start menu.

Figure 4. Start-Up Window

3.2.2 The Start-Up Window

When the software first executes, the user should see the Start-Up Window appear on the user's PC monitor. This window is shown in Figure 4. From this window, the user can navigate to three other main windows: the Conversion Window, the Data Collection Window, and CS5451A Pinout Diagram. (The CS5471 Pinout Diagram is included in a fourth window. Cirrus Logic's CS5471 device is very similar to CS5451A, except this device has only the first pair of voltage/current input channels.) To navigate to these windows, use the mouse to click on the "Menu" item, which is located towards the upper left corner of the Start-Up Window. "Menu" is a pull-down menu which contains four options. From this pull-down menu, the user can select any of the three windows mentioned above, and once this is done, the new window should appear. A fourth option called "Exit" should be selected when the user wants to terminate execution of the evaluation board software program.

If the user selects the "CS5451A Pinout Diagram" option in the "Menu" pull-down, the software will display a window which contains the pin diagram of the CS5451A. This pin diagram is included for the user's reference. Note that this window has no actual functionality.

The functionality of the Conversion Window and the Data Collection Window is described next.

3.2.3 The Conversion Window

Refer to Figure 5. After the user presses on the green-colored “START” button in this window, the software will begin to collect data for all six channels of the CS5451A. For each of the six channels, a certain number of continuous instantaneous data samples are bundled together. The period over which each bundle of samples is taken is called a “computation cycle.” The user controls the number of instantaneous data samples that will be taken (per channel) during one computation cycle by adjusting the number in the box labeled “Evaluation Software Cycle Count.” Note that the default value for this is set to 4000. Thus during every computation cycle, the PC software will acquire 4000 samples (from each of the six channels) and it will update the on-screen results of all six channels after calculating the results on each successive set of 4000 samples. The results that are displayed on this screen are therefore updated after each computation cycle. Note that the results of the very first computation cycle (after the “START” button has been activated) will not be valid. Accuracy of the Mean/Std. Dev/RMS results increases as the “Evaluation Software Cycle Count:” value is increased.

The user should understand how to interpret the values that are displayed in the 4x6 array of number boxes in the Conversion Window. The result values displayed in these 24 numeric output boxes are expressed on a normalized scale. The highest value (0.999...) represents the highest digital output code that can be issued from the CS5451A (which is +32767), while the lowest value -0.999... represents the lowest output code that can be issued from the CS5451A (which is -32768). This is because the CS5451A issues instantaneous output codes as two’s complement 16-bit words. Therefore, the range of values that can be returned from the CS5451A are between -32768 and +32767. The CS5451A issues instantaneous data, and every computation cycle, the software computes/displays the quantities which are described below:

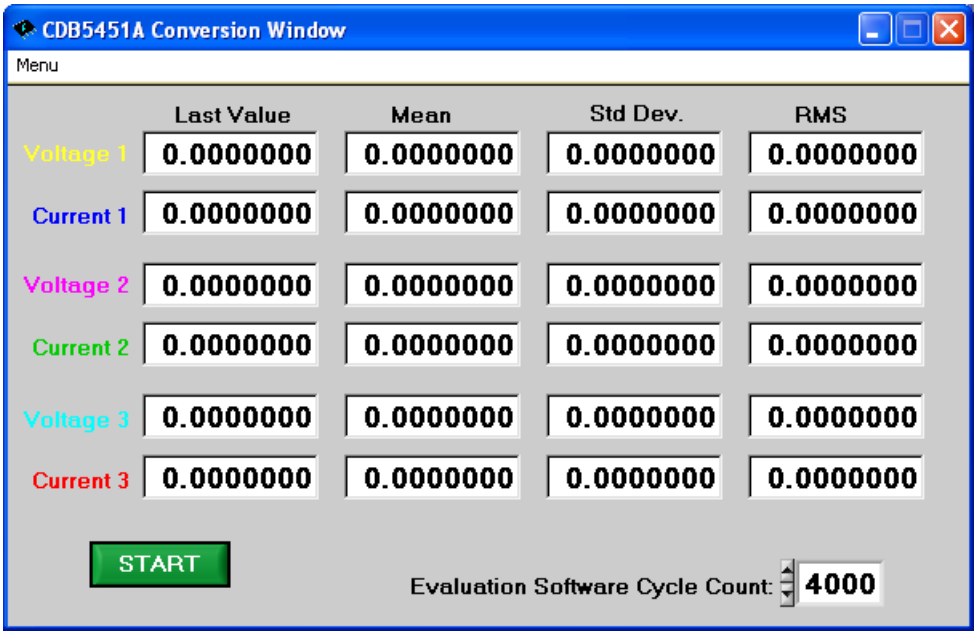


Figure 5. Conversion Window

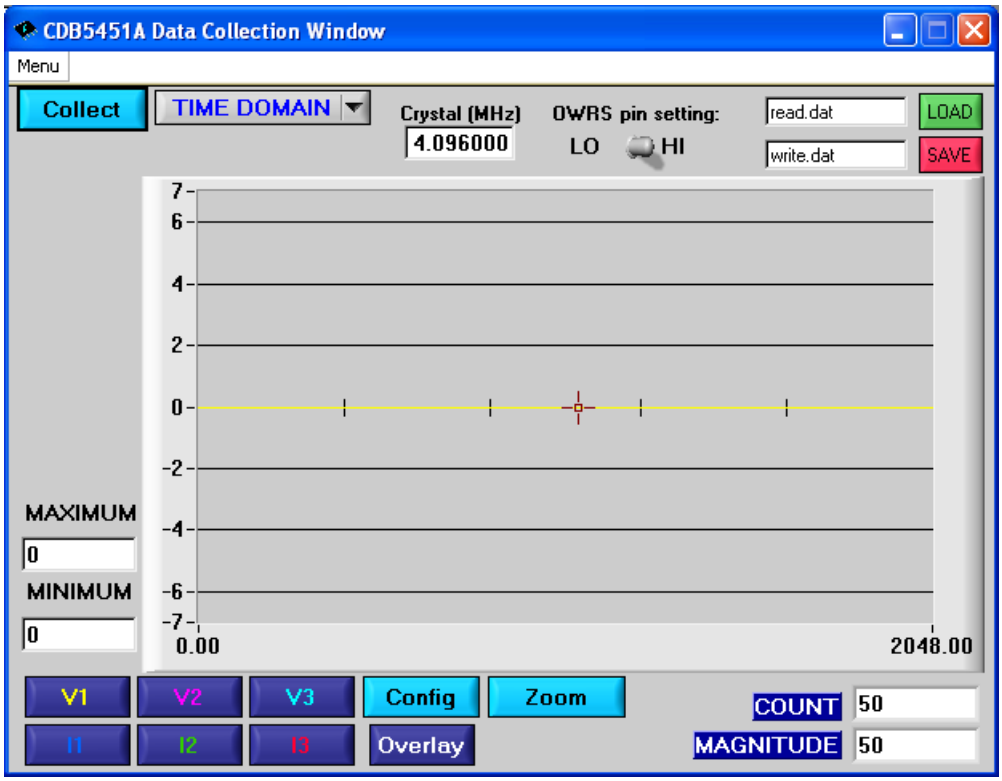


Figure 6. Data Collection Window (Time Domain)

3.2.3.1. Last Value

The first column is labelled as "Last Value." The value in this box represents the value of the very last instantaneous sample that was taken (for each channel) in the most recently-completed computation cycle. If the user's analog input waveforms are AC in nature, then this column of results will rarely have any meaning. But if the user applies a constant DC input signal to any of the analog input channels, then the Last Value column for that channel should display an output code that is relatively constant from one conversion cycle to the next.

3.2.3.2. Mean

The values in this column represent the simple average of the sample values in the latest computation cycle.

3.2.3.3. Std Dev.

The values in this column represent the computed standard deviation over the set of values in the most recent computation cycle.

3.2.3.4. RMS

The values in this column represent the computed RMS value over the most recently-completed computation cycle.

3.2.4 Data Collection Window

The Data Collection Window (Figs 6, 8, and 9) allows the user to collect samples sets of data from CS5451A and analyze them using time domain, FFT, and histogram plots. The Data Collection Window is accessible through the Menu option, or by pressing F4.

3.2.4.1. Collect Button

This button will collect data from the CS5451A, to be analyzed in the plot area. See the section on Collecting Data Sets for more information.

3.2.4.2. Time Domain / FFT / Histogram Selector

This selector button is located just to the right of the Collect Button. The label on this button will change as the user selects which analysis is to be performed ("Time Domain" or "FFT" or "Histogram"). When the software is first started, the default mode on this selector button is Time Domain. This user should click on this button to select which type of data processing to perform on the collected data and display in the plot area. Refer to the section on Analyzing Data for more information.

3.2.4.3. "Crystal" Value Indicator Box

The value in this box reflects the frequency of the CS5451A's clock input (at the XIN pin). Since the XIN frequency affects the sampling rate (the output word rate) of the CS5451A, this information must be specified to the software so that it can accurately depict the frequency-content of the sampled data (in Hz) when performing an FFT analysis. The user can enter the crystal frequency that is used on the CDB5451A board into this box. The default value of this box is set for the on-board 4.096MHz oscillator.

3.2.4.4. OWRS Pin Setting:

This switch should be adjusted whenever the user toggles the S1-1 DIP switch (on the evaluation board). The default setting of this switch is HI, corresponding to the default setting on S1-1 (default setting is "OPEN"). S1-1 drives the CS5451A's OWRS pin to logic "1". A logic "1" on OWRS sets the sampling frequency of all six CS5451A input channels to XIN/1024. To toggle the state of the on-screen switch, simply click on the switch with the mouse.

3.2.4.5. Config Button

This button will bring up the configuration window (shown in Fig 7) in which the user can modify the data collection specifications. See the discussion of the Config Window in this document.

3.2.4.6. Save Button

The red-colored SAVE button will save the data in the current plot to a file. The exact path and filename can be specified by the user in the text window located just to the left of the SAVE button. The data collected for all six channels will be saved to a text file.

3.2.4.7. Load Button

The green colored LOAD button will load any data file that was previously generated by clicking on the red SAVE button. The exact path and filename must be specified by the user in the text window located just to the left of the LOAD button.

3.2.4.8. Channel Selector Buttons

Clicking on six buttons labeled as "V1" "V2" "V3" and "I1" "I2" "I3" will display a certain channel of data. "V1" refers to the data taken from the Vin1+/Vin1- input pins of the CS5451A. This is similar for "V2" and "V3". In a similar manner, clicking on the "I1" "I2" "I3" buttons will display the voltage measured across the first, second, and third pairs of current channel input pins (designated as IinA+/IinA- for A = 1, 2, 3).

3.2.5 Config Window

See Figure 7. Clicking on the Config button will bring up a small pop-up window called the Config Window. The Config Window allows the user to set up the data collection and analysis parameters, which are described next.

3.2.5.1. Number of Samples

This box allows the user to select the number of samples to collect. The user can choose any whole-number power of 2 between 16 and 32768.

3.2.5.2. Average

When performing FFT processing, this box will determine the number of FFTs to average. FFTs will then be collected and averaged when the user clicks on the Collect Button.

3.2.5.3. FFT Window

This box allows the user to select the type of windowing algorithm for FFT processing. Windowing algorithms include the Blackman, Black-Harris, Hanning, 5-term Hodie, and 7-term Hodie. The 5-term Hodie and 7-term Hodie are windowing algorithms developed at Cirrus Logic.

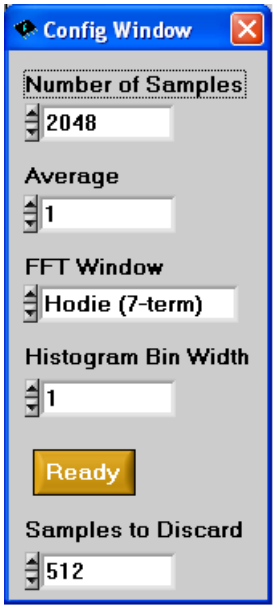


Figure 7. Configuration Window

3.2.5.4. Histogram Bin Width

This box allows for a variable "bin width" when plotting histograms of the collected data. Each vertical bar in the histogram plot will contain the number of output codes contained in this box. Increasing this number may allow the user to view histograms with larger input ranges.

3.2.5.5. Samples to Discard

This number represents the number of CS5451A sample periods that will be ignored before the software starts to collect samples (when the user presses on the Collect Button). After the software has skipped over this many data samples, the software will then begin to save samples from the device (for all six channels). The number of samples that are actually saved is equal to the number specified in the Number of Samples box.

3.2.5.6. Ready Button

After the user has adjusted the parameters in the Config Window to the desired settings, the user must click on the READY button to close the Config Window and return to the Data Collection Window.

3.2.5.7. Crystal (MHz)

This frequency value is used to properly perform the FFT operation on a set of collected data. The user can adjust this value. Default value is 4.096 (Mhz), which is the frequency of the crystal oscillator (U1) on the evaluation board.

3.2.6 Analyzing Data

The evaluation software provides three types of analysis tests - Time Domain, Frequency Domain, and Histogram. The Time Domain analysis processes acquired conversions to produce a plot of Output Code versus Conversion Sample Number. The Frequency Domain analysis processes acquired conversions to produce a magnitude versus frequency plot using the Fast-Fourier transform (results up to Fs/2 are calculated and displayed). The Histogram analysis test processes acquired conversions to produce a histogram plot. Statistical noise calculated are also calculated and displayed.

3.2.7 Time Domain Information

The following controls and indicators are associated with the Time Domain Analysis. Time domain data can be plotted in the Data Collection Window by setting the Time Domain / FFT / Histogram selector to "Time Domain."

3.2.7.1. Count

Displays current x-position of the cursor on the time domain display.

3.2.7.2. Magnitude

Displays current y-value of the cursor on the time domain display.

3.2.7.3. Maximum

Indicator for the maximum value of the collected data set.

3.2.7.4. Minimum

Indicator for the minimum value of the collected data set.

3.2.8 Frequency Domain Information

The following section describes the indicators associated with Fast Fourier Transform (FFT) analysis. FFT data can be plotted in the Data Collection Window by setting the Time Domain / FFT / Histogram selector button to “FFT.”

3.2.8.1. Frequency

Displays the x-axis value of the cursor on the FFT display.

3.2.8.2. Magnitude

Displays the y-axis value of the cursor on the FFT display.

3.2.8.3. S/D

Indicator for the Signal-to-Distortion Ratio, 4 harmonics are used in the calculations (decibels).

3.2.8.4. SINAD

Indicator for the Signal-to-Noise + Distortion Ratio (decibels).

3.2.8.5. SNR

Indicator for the Signal-to-Noise Ratio, first 4 harmonics are note included (decibels).

3.2.8.6. S/PN

Indicator for the Signal-to-Peak Noise Ratio (decibels).

3.2.8.7. FS-PdB

Not using windowing, how far down from zero the peak voltage input value is (decibels).

3.2.9 Histogram Information

The following is a description of the indicators associated with Histogram Analysis. Histogram can plotted in the Data Collection Window by setting the Time Domain / FFT / Histogram selector to “Histogram.”

3.2.9.1. Bin

Displays the x-axis value of the cursor on the Histogram.

3.2.9.2. Magnitude

Indicator for the maximum value of the collected data set.

3.2.9.3. Mean

Average value of the collected data set.

3.2.9.4. Variance

Indicator for the calculated variance of the collected data set.

3.2.9.5. STD_DEV

Indicator for the calculated standard deviation of the collected data set.

3.2.9.6. Maximum

Indicator for the maximum value of the collected data set.

3.2.9.7. Minimum

Indicator for the minimum value collected in the data set.

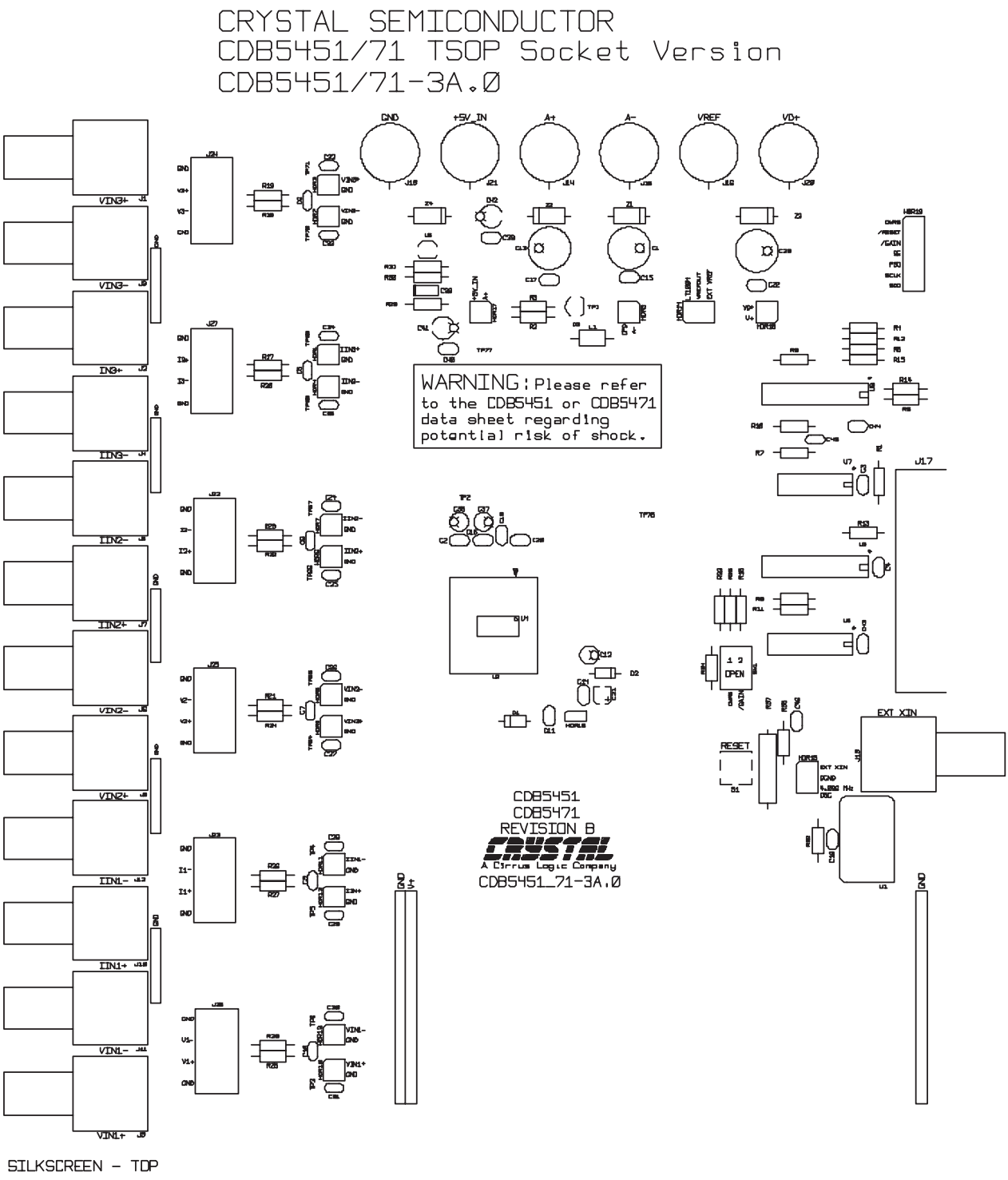


Figure 8. Silkscreen

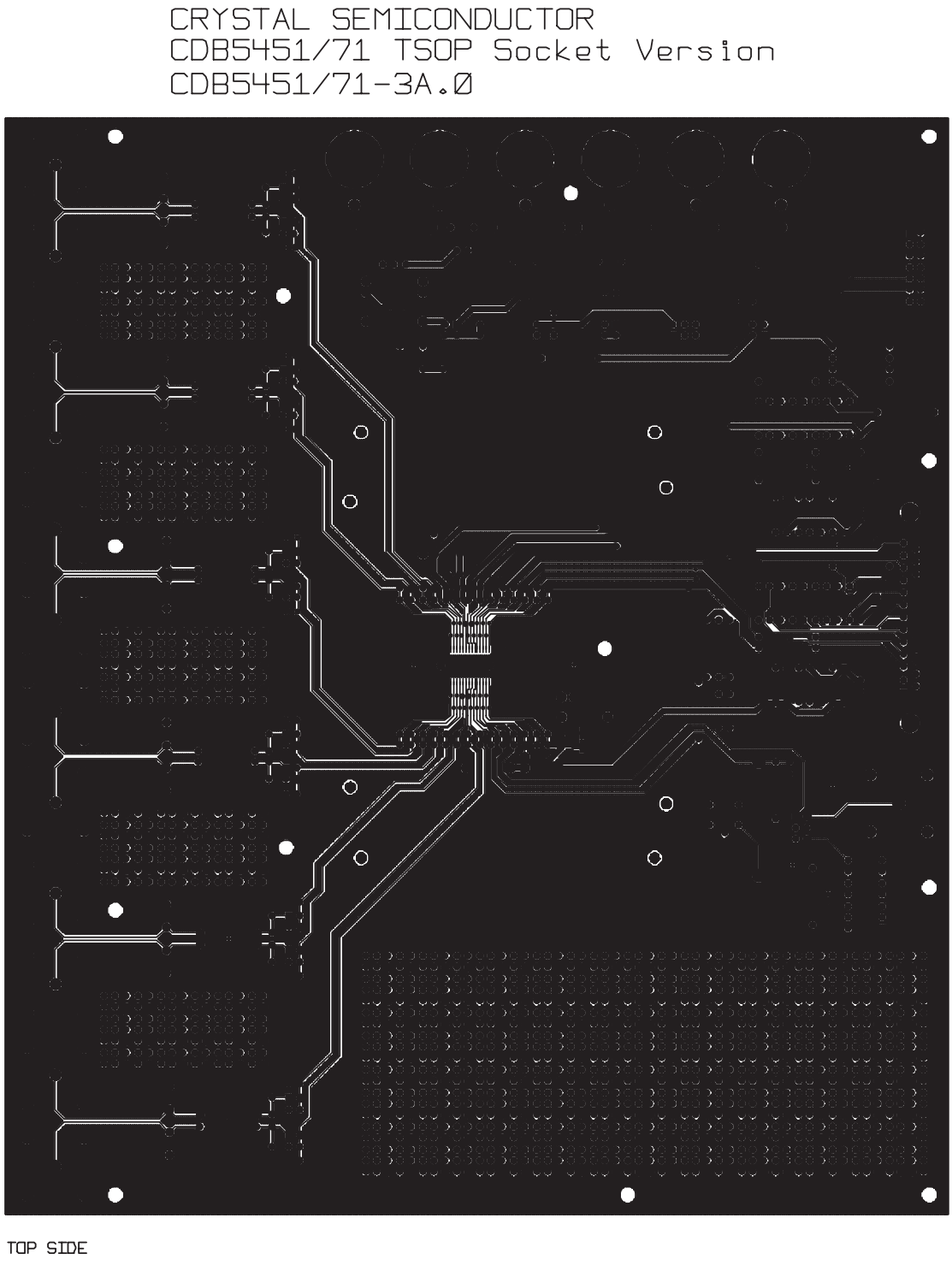


Figure 9. Circuit Side

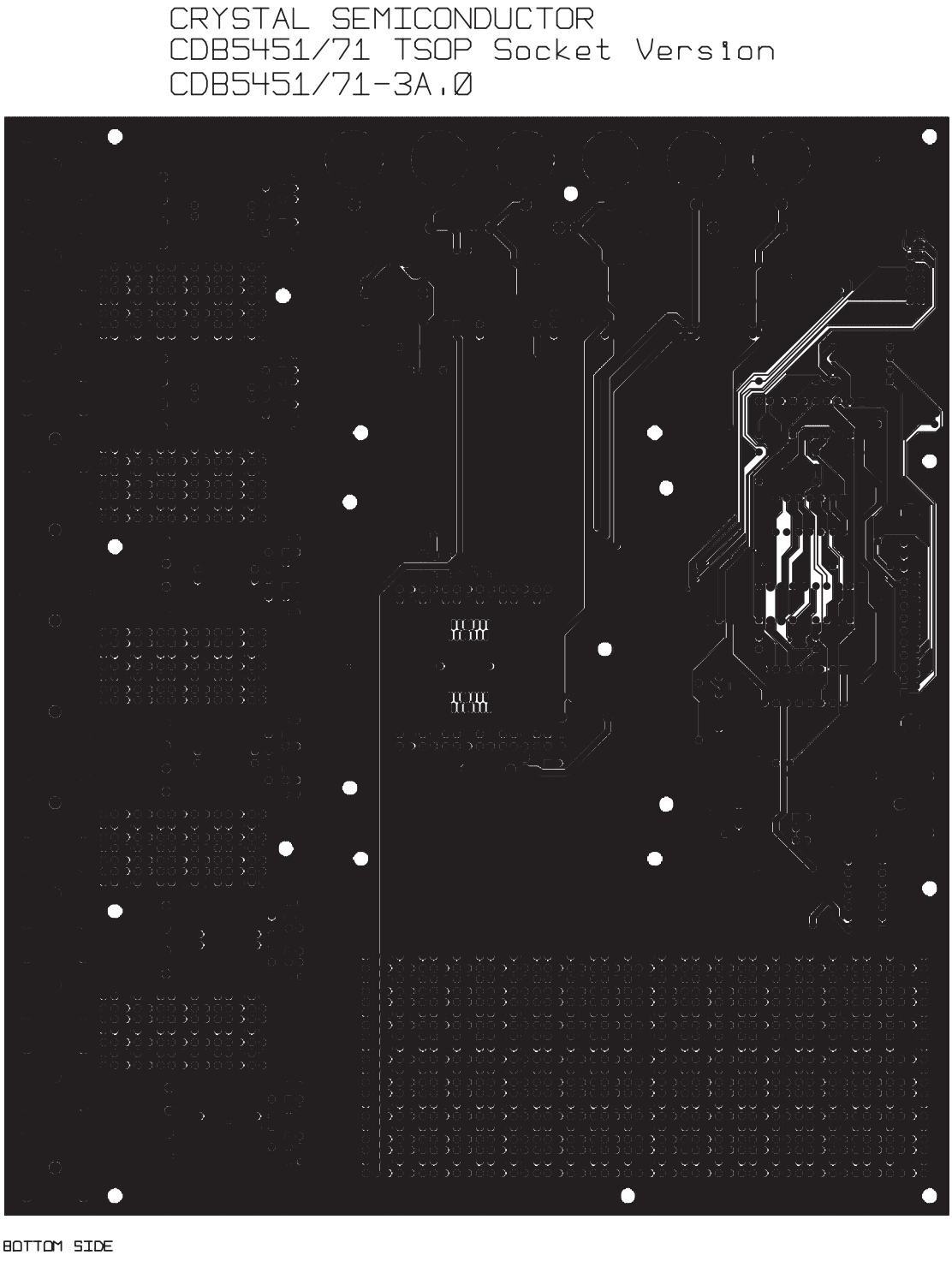


Figure 10. Solder Side

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to **www.cirrus.com**